Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A pulse interval to voltage converter, comprising:
a delay unit for delaying an input pulse signal;
a counter connected to the delay unit, wherein the count of the counter is reset to zero when the counter receives the input pulse signal;
a latch for locking the count of the counter before the counter is reset; and
a digital-to-analog converter for converting the count of the latch into an analog signal.

[c2] The pulse interval to voltage converter of Claim 1, further comprising a frequency regulator for regulating a clock frequency of a clock generator.

[c3] The pulse interval to voltage converter of Claim 1, further comprising a clock generator for generating clock signals.

[c4] The pulse interval to voltage converter of Claim 2, wherein the frequency regulator is a frequency divider.

[c5] The pulse interval to voltage converter of Claim 1, further comprising a synchronization unit for synchronizing the input pulse signal and a clock signal.

[c6] The pulse interval to voltage converter of Claim 1, further comprising an underflow protection circuit for preventing the delay unit from receiving other input pulse signals when the delay unit delays the input pulse signal.

[c7] The pulse interval to voltage converter of Claim 1, further comprising an overflow protection circuit for ignoring the count of the counter when the counter exceeds a predetermined value.

[c8] The pulse interval to voltage converter of Claim 1, further comprising a conditioning unit for regulating the input pulse signal to conform to transistor-transistor logic (TTL) specification.

[c9] The pulse interval to voltage converter of Claim 1, wherein the delay unit comprises two counters of integrated circuit (IC) type and a NOR gate.

[c10] The pulse interval to voltage converter of Claim 9, wherein the delay unit further comprises four digital dials, the digital input of each counter of IC type is incorporated with two of the digital dials for setting.

[c11] The pulse interval to voltage converter of Claim 4, wherein the frequency divider comprises two counters of IC type, a NOR gate and an inverter.

[c12] The pulse interval to voltage converter of Claim 11, wherein the frequency divider further comprises four digital dials for setting.

[c13] A pulse interval to voltage conversion method, comprising the steps of:
(a) delaying an input pulse signal;
(b) calculating the time between the input pulse signal and its preceding delayed input pulse signal;
(c) converting the time into a digital voltage; and
(d) converting the digital voltage into an analog voltage.

[c14] The pulse interval to voltage conversion method of Claim 13, wherein the time calculation in step (b) is based on the number of clock cycles between the input pulse signal and its preceding delayed input pulse signal.

[c15] The pulse interval to voltage conversion method of Claim 13, further comprising a step of decreasing the frequency of a clock signal.

[c16] The pulse interval to voltage conversion method of Claim 13, further comprising a step of ignoring other input pulse signals when the input pulse signal is being delayed.